**S. Y. B. Tech (EE)**

**Trimester: IV Subject:** Analog and Digital Integrated Circuits

**Name: Class:**

**Roll No: Batch:**

**Experiment No: 09**

|  |  |
| --- | --- |
| **Marks** | **Teachers Signature with Date** |
|  |  |
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**Name of the Experiment**: **Design and implement Sequence Detector.**

**Performed on:**

**Submitted on:**

**Aim: Design and implement Sequence Detector.**

A) Design a sequence detector to detect the bit sequence of ..110… using Mealy Machine.

**Prerequisite:**

* Concept of Synchronous sequential Circuits
* Basics of Finite State Machines

**Objectives:**

* To learn and design Finite State Machines
* To design and implement Sequence Detector

**Components and equipment required:**

Multisim/DeldSim Simulator/Digital trainer kit, Connecting probes, ICs 7476 and logic gates ICs like 74LS08 etc.

**Theory:**

**Finite State Machines:**

The clocked sequential circuit is synchronous circuit. In clocked synchronous circuit, the flip-flops are the basic elements. All the flip-flops those are used in circuit are clocked simultaneously. The next state of clocked synchronous circuits depends on present input (s) and present state of clocked circuits. The output of clocked synchronous circuit may or may not be function of present input; therefore the clocked synchronous circuits are classified into two types such as 1) Moore circuit and 2) Mealy circuit. Sequential Circuits with finite number of states are called as Finite State Machines (FSM)

**Moore Machines:**

A finite state machine, whose output is a function of the present state only. Moore model requires more number of states for implementing the function.

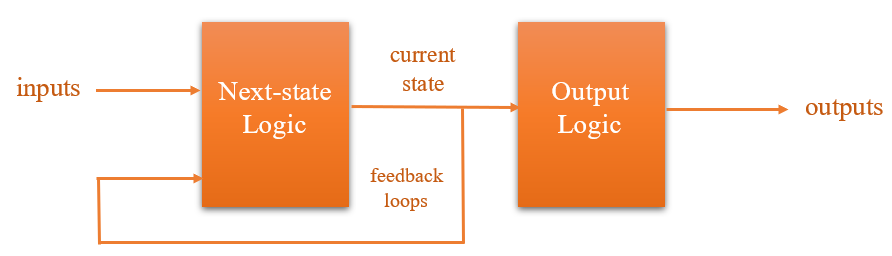


Figure 9.1: Moore Machine general Block Diagram

**Mealy Circuit:**

A finite state machine, whose output is a function of the present state and the present input. It requires less number of states for implementing the function.

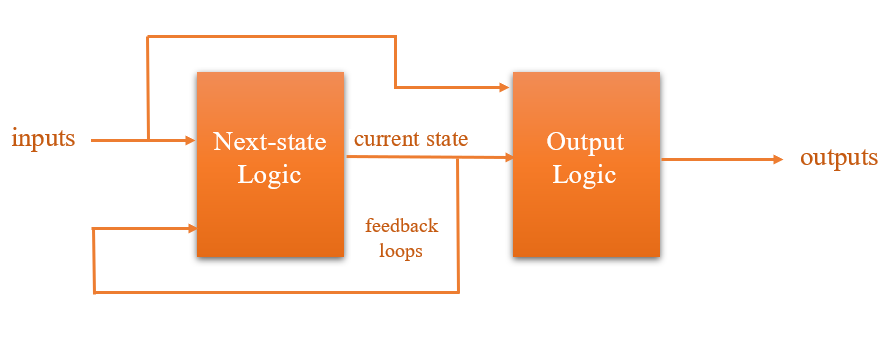


Figure 9.2: Melay Machine general Block Diagram

**Sequence detector:**

A sequence detector is a sequential state machine that takes an input string of bits and generates an output 1 whenever the target sequence has been detected. In a Mealy machine, output depends on the present state and the external input (x). Hence, in the diagram, the output is written outside the states, along with inputs. Sequence detector is of two types:

Overlapping

Non-Overlapping

In an overlapping sequence detector, the last bit of one sequence becomes the first bit of the next sequence. However, in a non-overlapping sequence detector, the last bit of one sequence does not become the first bit of the next sequence.

Examples:

For non-overlapping case

Input :0110101011001

Output:0000100010000

For overlapping case

Input :0110101011001

Output:0000101010000

**Design of Sequence Detector:**

**Step 1: Draw State diagram:** Sequence detector 110 Mealy Machine

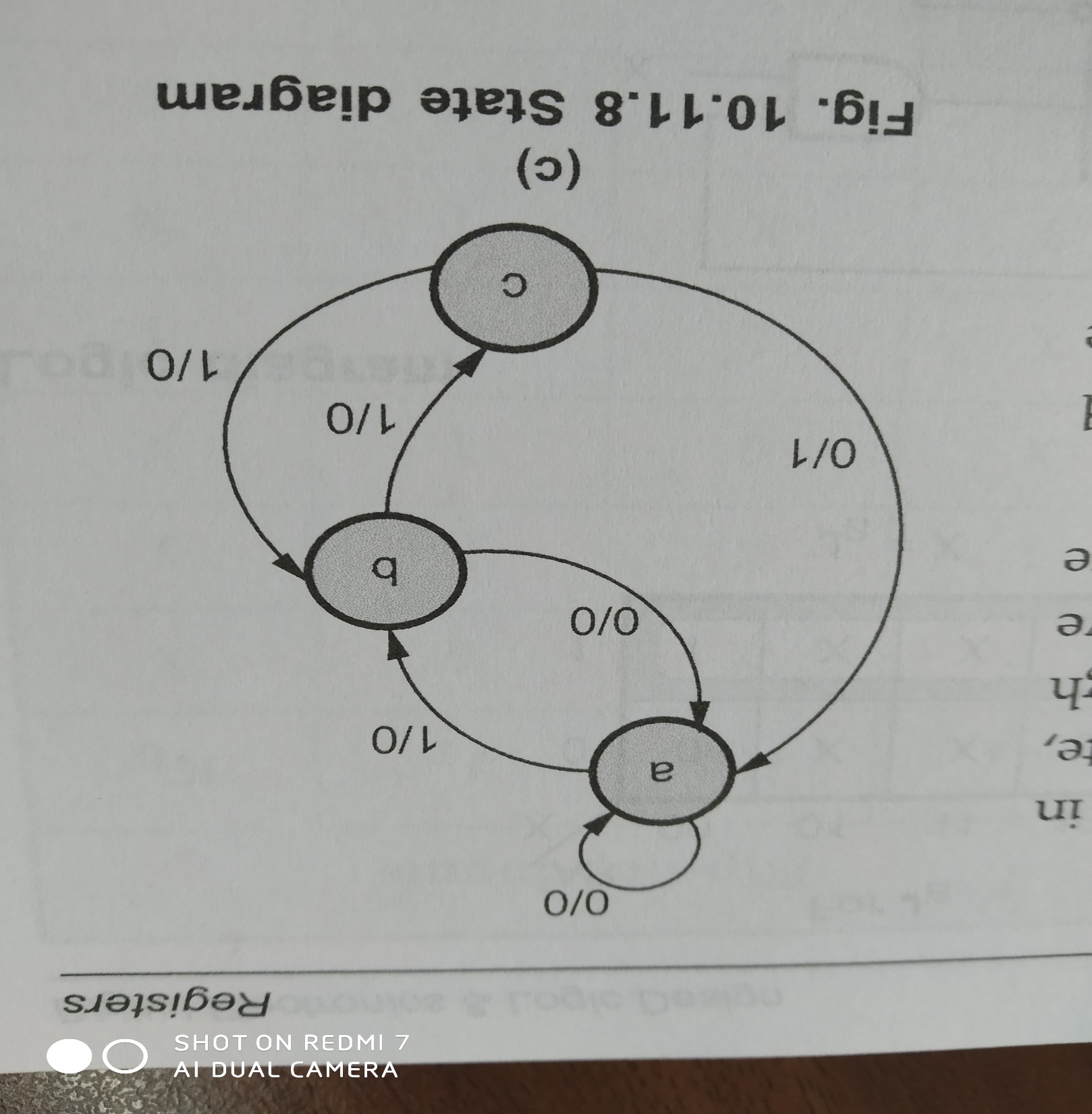
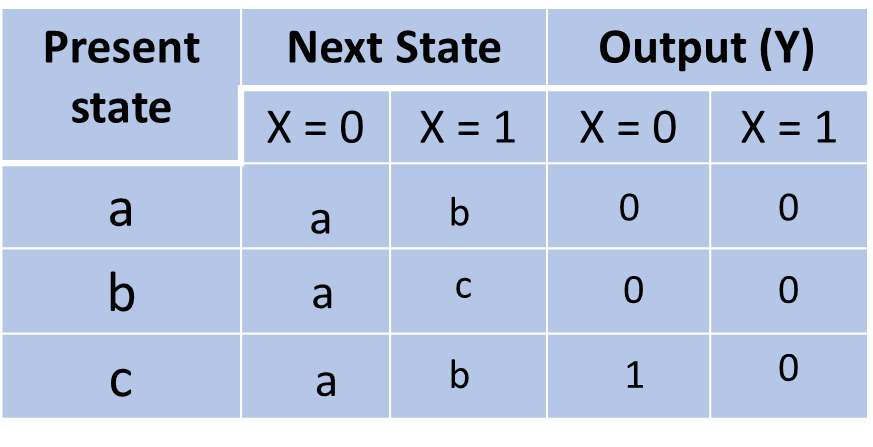
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Figure 9.3: Melay Machine for 110

**Step 2:**

**State Table: Sequence detector 110**

Consider Input = X and Output = Z

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Check if state reduction is required. As no two rows of next state and output in the state table are same, state reduction is not required in this design.

**Step 3: State assignment:** Sequence detector 110

State assignment

a = 00 b = 01 c = 10

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Present**  **state** | **Next State** | | **Output** | |
| **X = 0** | **X = 1** | **X = 0** | **X = 1** |
| **00** | **00** | **01** | **0** | **0** |
| **01** | **00** | **10** | **0** | **0** |
| **10** | **00** | **01** | **1** | **0** |

Let us call MSB flip flop as A And LSB flip flop as B

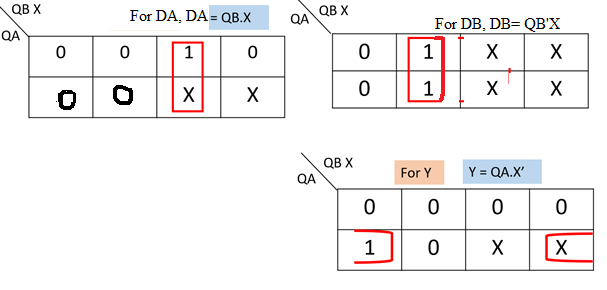
Input = X

Output = Y

**Step 4:Prepare state transition table**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Present State 00** | | **Input** | **Next State** | | **Flip Flop Inputs** | | | | **Output** |
| **QA** | **QB** | **X** | **QA+1** | **QB+1** | **DA** |  | **DB** |  | **Y** |
| 0 | 0 | 0 | 0 | 0 | 0 |  | 0 |  | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |  | 1 |  | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |  | 0 |  | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |  | 0 |  | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |  | 0 |  | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 |  | 1 |  | 0 |
| 1 | 1 | 0 | X | X | X |  | X |  | X |
| 1 | 1 | 1 | X | X | X |  | X |  | X |

**Step 5: K-maps: Sequence detector 110**

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**Step 6: Circuit Diagram: Sequence detector 110**

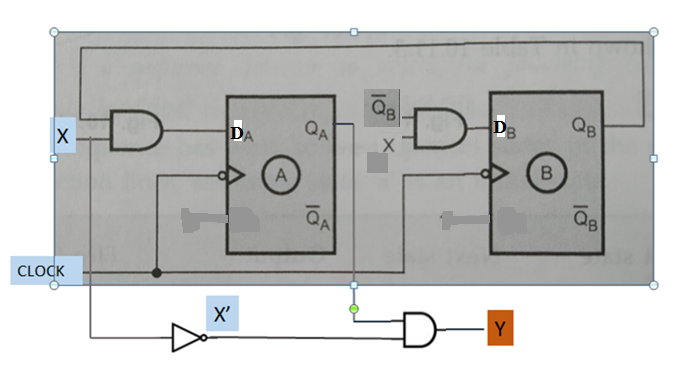
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Figure 9.4: Melay Machine circuit diagram for sequence detector

**Applications of Sequence Detectors:**

1. In the decoding equipment to provide “flags” which indicate the beginning (or end) of a data block (e.g., a TV frame).
2. ALU, microprocessors and DSP.

**Design and implementation:**

1. Implement a sequence detector to detect the bit sequence of ..110… using Mealy Machine

**Procedure:**

1. Design Sequential circuit logic circuit as per given problem statement.
2. Connect the IC 74LS76 and other basic logic gate ICs as per diagram.
3. Give VCC supply and ground connection to each IC.
4. Give clock to all D FFs.
5. Observe the output and verify the truth table.

**Conclusion:**

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**Post Lab Questions:**

1. What is Sequence Detector?
2. What does Arc/Arrow pointer in Mealy machine state diagram signify?
3. Sequence detector is a synchronous or asynchronous circuit? Comment

**Additional links for more information:**

* + - 1. https://www.youtube.com/watch?v=NDtOh3XClDc&list=RDCMUC640y4UvDAlya\_WOj5U4pfA&index=1
      2. <https://mddl-iitb.vlabs.ac.in/sequence_detector/index.html>
      3. https://de-iitr.vlabs.ac.in/exp/truth-table-gates/theory.html